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Enabling Gate Dielectric Design for All Solution-Processed, High-Performance, Flexible Organic Thin-Film Transistors

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Solution processabilities of both active and passive materials (conductor, semiconductor, and dielectric) for organic thin-film transistors (OTFTs) are crucial to the fabrication of printed, integrated, transistor circuits. The possibility of using low-cost solution patterning and deposition techniques, coupled with such salient OTFT circuit features of being physically compact, lightweight, and flexible, has fuelled the current surge in organic electronics research.¹ While there exist many printable and functionally capable semiconductors^{2,3} and conductors,⁴ few solution-processable and electrically satisfactory dielectric materials⁵ are available to enable design of flexible electronics.

The interfacial interactions of organic semiconductor layer with gate dielectric are often very specific and play a decisive role in the functioning of field effect transistor (FET) devices. Optimum device performance generally requires synergistic interactions at the semiconductor/dielectric interface. For example, while the octyltrichlorosilane (OTS-8) self-assembled monolayer (SAM) on a thermal SiO₂ surface enhances the semiconductor performance of regioregular polythiophene, PQT-12,^{2a} utilization of an untreated native SiO₂ surface has led to reductions in mobility and on/off ratio by as much as up to 3 orders of magnitude.⁶ A great variety of other alkyl silylating agents have also been explored with the objective of optimizing the dielectric/semiconductor interactions, often with satisfactory performance results.⁷⁻¹¹ Specifically, hexamethyldisilazane (HMDS) surface treatment has been employed to promote segregation of regioregular polythiophenes for improved mobility.⁷ while perfluorosilane modification has been used for manipulating threshold voltages of OTFTs.^{8,9} More recently, alkylphosphonic acid SAM on alumina has been demonstrated to be effective in achieving, hitherto, the best FET performance of evaporated pentacene semiconductor.¹¹ However, all of these modifications have two limiting characteristics. First, the creation of a synergistic dielectric surface requires appropriate chemical reactions between the modification agent and the dielectric surface. Second, if SAMs are utilized, their qualities, which depend critically on the dielectric surface chemistry and the methods through which they are formed, would greatly affect the final FET performance. These modification approaches may thus be difficult to implement reproducibly in high-throughput manufacturing processes, particularly on such chemically inert surfaces as those of common plastic substrates for electronic design.

In this communication, we report an effective approach to a solution-processed dielectric design to enable all solution-processed, high-performance OTFTs for flexible electronic applications. This is through a dual-layer dielectric structure comprising a UV-cross-linked poly(4-vinyl phenol-*co*-methyl methacrylate) (PVP–PMMA) bottom layer and a thermally cross-linked polysiloxane top layer of, for example, poly(methyl silsesquioxane) (pMSSQ)



Figure 1. Schematic depiction of formation of poly(methyl silsesquioxane) from methyltrimethoxysilane and its incorporation as a dielectric top layer in an all-solution processed organic thin film transistor device on PET.

which can be readily generated from methyltrialkoxysilane.¹² The partially cross-linked pMSSQ in an appropriate solvent is solution processable, and its solution viscosity can be adjusted to suit various solution deposition techniques such as spin coating, stamping, flexography, and inkjet printing to name a few. After deposition, the pMSSQ layer can then be fully cross-linked thermally at a temperature which is compatible with common commercial plastic substrates for fabrication of flexible integrated circuits.

Figure 1 schematically depicts the preparation of pMSSQ and its use in modifying the PVP-PMMA surface for an all solutionprocessed OTFT on a polyester plastic substrate (PET) such as Mylar. A thin gold film serving as the gate electrode was first formed on a PET substrate by spin coating a gold nanoparticle dispersion, followed by annealing at 150 °C.4a A solution of PVP-PMMA in DMF was spun cast on top of this gold film and crosslinked via exposure to a 254-nm UV light. Thereafter, a 50-nm pMSSQ layer was laid on top of cross-linked PVP-PMMA by spin coating a solution of pMSSQ in methyl isobutyl ketone, followed by curing at 140-160 °C. This was followed by patterning an array of gold source/drain electrode feature pairs via stencil printing using a gold nanoparticle dispersion, followed by annealing at 150 °C.4a Finally, a semiconductor layer was deposited using the PQT-12 nanoparticle dispersion via spin coating or inject printing,¹³ thus creating a series of OTFTs of different channel length/width dimensions. For comparison, OTFT devices without pMSSQ top layers were also fabricated. All the devices were annealed at 140 °C to achieve optimum molecular ordering in the PQT-12 semiconductor layer for best OTFT performance.

The surface properties of dielectrics were characterized by water advancing contact angle measurement. The uncoated PVP–PMMA surface, with a high concentration of surface hydroxy groups, was hydrophilic and exhibited a water contact angle of \sim 78°. After treatment with pMSSQ, a hydrophobic surface with a water contact angle of \sim 98° was obtained (Table 1). This contact angle is identical

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Table 1. Water Contact Angle and Device Performance of the OTFTs with Different dielectrics.

gate dielectric	contact angle	mobility (cm ² /V.s)	on/off ratio	$V_{th}\left(V ight)$
PVP-PMMA	$78\pm3^{\circ}$	0.003	10^{4}	-4
PVP-PMMA/OTS-8	$95 \pm 3^{\circ}$	0.003	10^{4}	-4
PVP-PMMA/pMSSQ	$98\pm2^{\circ}$	0.15	10^{6}	-2



Figure 2. (a) Source-drain current versus source drain voltage at different gate voltages for an OTFT with dual-layer gate dielectric. (b) Source-drain current versus gate voltage at a source-drain voltage of -60 V for OTFTs with different gate dielectrics: dual-layer dielectric, black line; OTS-8modified UV cured-PVP-PMMA dielectric, blue line; UV-cured PVP-PMMA dielectric, red line. (Channel length = 90 μ m; channel width = 1000 µm).

to the case when a hydrophilic native SiO₂ surface is modified with octyltrichlorosilane (OTS-8).6 Modification of the PVP-PMMA dielectric surface with OTS-8 gave a water contact angle of $\sim 95^{\circ}$, but the contact angle decreased to about 80° in a few hours, indicative of the instability of OTS-8 SAM on PVP-PMMA surface.

All the OTFT devices were fabricated under ambient conditions and evaluated using a Keithley SCS-4200 in a black metal box in air. Figure 2 shows the output and transfer curves of all-solution processed OTFTs on PET substrates. The devices with the nonmodified, UV-cured PVP-PMMA dielectric showed a mobility of 0.003 cm² V⁻¹ s⁻¹ and current on/off ratio of 10⁴. With OTS-8 modification, the devices gave similar results. However, with the present dual-layer gate dielectric i.e., UV-cured PVP-PMMA modified with pMSSQ (dielectric constant = 4.0; capacitance = 9.0 nF cm⁻²), the OTFTs exhibited ideal FET behaviors, conforming well to the conventional transistor models in both the linear and saturated regimes. The output characteristics showed no observable contact resistance, very good saturation behavior, and clear saturation currents which were quadratic to gate bias. The devices switched on at ~ 0 V, displayed subthreshold slopes of ~ 2 V dec⁻¹, and exhibited small hysteresis effect. Compared with the devices with the nonmodified or OTS-8-modified UV-cured PVP-PMMA dielectrics, the improvements were phenomenal, with mobility improved by as much as 50 times to 0.15 cm² V⁻¹ s⁻¹ and on/off ratio by 2 orders of magnitude to 10⁶ (Table 1). The performance characteristics of these OTFTs were very consistent and reproducible, with little transistor-to-transistor variations, which would be critically important for large-area electronic device fabrication where large OTFT circuits with hundreds of thousands of transistors may be involved.

The use of just pMSSQ as gate dielectric gave very low device yields, and its coupling with a chemically cross-linked PVP-PMMA dielectric led to high gate leakage currents. The observed

low gate leakage with the UV-cross-linked PVP-PMMA gate dielectric is attributable to a much higher cross-link density.

The current pMSSO/UV-cured PVP-PMMA dual-layer gate dielectric is robust and extremely resistant to common organic coating solvents including alcohol, toluene, chlorinated solvents such as chloroform, chlorobenzene, dichlorobenzene, etc. Subsequent liquid deposition of the semiconductor layer followed by annealing did not lead to its dimensional and structural damages or adverse electrical performance consequences.

In conclusion, we have concretely demonstrated that the pMSSQ/ UV-cured PVP-PMMA dielectric is a solution-processable, highperformance dielectric that is suitable for all printed OTFT circuits on flexible substrates.

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Supporting Information Available: Instrumentation, synthesis of the pMSSQ, capacitance measurement. This material is available free of charge via the Internet at http://pubs.acs.org.

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